**POORNIMA UNIVERSITY, JAIPUR.**

**END SEMESTER EXAMINATION, November 2022**

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|  | **2BT3178** | Roll No. | Total Printed Pages: 2 |
| **2BT3178** |  |
| B. Tech. II Year III-Semester (Back) End Semester Examination, November 2022  **(AI / DS)** | |
| **BAI03108 / BDS03108 : Digital Electronics** | | | |

# Time: **3** Hours. Total Marks: **60**

Min. Passing Marks: **21**

Attempt **five** questions selecting one question from each Unit. There is internal choice from Unit I to Unit V. Marks of each question or its parts are indicated against each question / parts. Draw neat sketches wherever necessary to illustrate the answer. Assume missing data suitably (if any) and clearly indicate the same in the answer.

Use of following supporting material is permitted during examination for this subject.

# **1.--------------------------Nil--------------------** **2.------------------Nil-----------------------**

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|  |  | **UNIT-I (CO1)** | **Marks** | **Bloom Level** |
| **Q.1** | **(a)** | Solve the following:   1. Hexadecimal Number (1E.53)16 Into Octal 2. Octal Equivalent of The Decimal Number (417)10 3. Convert (214)8 Into Decimal 4. Binary Number (01011.1011)2 Into Decimal. 5. (0.345)10 Into an Octal Number. 6. Octal To Binary Conversion: (24)8 =? | **(6)** |  |
|  |  |  |  |  |
|  | **(b)** | Using a Karnaugh map, simplify the following Boolean expression for Y into a product of sums (POS) form  Y = C(ABD + D)’ + ABC + D. | **(6)** |  |
|  |  | **OR** |  |  |
| **Q.2** | **(a)** | Simplify the following four variable function F (A, B, C, D) using the K-map method:  Minterms: A.B.C.D, A.B.C.D, A.B.C.D, A.B.C.D, A.B.C.D, A.B.C.D  Don’t cares: A.B.C.D, A.B.C.D, A.B.C. D | **(6)** |  |
|  |  |  |  |  |
|  | **(b)** | Use a K map to simplify:  1. F(P,Q,R,S)=∑(0,2,5,7,8,10,13,15)  2. F(A,B,C)=π(0,3,6,7)  3. y = C(ABD + D) + ABC + D. | **(6)** |  |
|  |  | **UNIT-II (CO2)** |  |  |
| **Q.3** | **(a)** | The logic functionality realized by the circuit shown below is? Explain in detail the working of this circuit using CMOS logic. | **(6)** |  |
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|  | **(b)** | Realise the following Boolean functions:  X=(AB+CD)’ using CMOS logic  X=AB+C using PMOS logic | **(6)** |  |
|  |  | **OR** |  |  |
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| **Q.4** | **(a)** | What do you understand by following properties of logic families?  (i) Fan Out (ii) Figure Of Merit (iii) Noise Margin (iv) Current Mode Logic | **(6)** |  |
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|  | **(b)** | Explain the construction and working of a CMOS logic, also implement the NAND & NOR logic gate using NMOS logic gate. | **(6)** |  |
|  |  | **UNIT-III (CO3)** |  |  |
| **Q.5** | **(a)** | Draw and explain the logic diagram for binary adder and subtractor. | **(6)** |  |
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|  | **(b)** | Implement the following and explain the working:  (i) Full adder using Half adder (ii) F (A, B, C) =m (0,4,6,7) using 2x1 Mux | **(6)** |  |
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| **Q.6** | **(a)** | Design a logic circuit that has three inputs, A, B, and C, and whose output will be HIGH only when a minority of the inputs are HIGH. | **(6)** |  |
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|  | **(b)** | Identify the circuit given below and explain it properly | **(6)** |  |
|  |  | **UNIT-IV (CO4)** |  |  |
| **Q.7** | **(a)** | What do you understand by race around condition, how is it over come in master slave configuration? | **(6)** |  |
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|  | **(b)** | Write a short note on shift registers | **(6)** |  |
|  |  | **OR** |  |  |
| **Q.8** | **(a)** | Draw and explain the four-bit ripple counter diagram using flip flop that trigger on positive edge. | **(6)** |  |
|  |  |  |  |  |
|  | **(b)** | Explain the construction and working of a NAND gate SR flip flop. | **(6)** |  |
|  |  | **UNIT V (CO5)** |  |  |
| **Q.9** | **(a)** | Write a short note on the following:  (i) Memory Hierarchy (ii) PLA | **(6)** |  |
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|  | **(b)** | What are the types of RAM & ROM, describe in detail | **(6)** |  |
|  |  | **OR** |  |  |
| **Q.10** | **(a)** | Explain in detail about PLA with the help of an example, also sate how its is different from PAL | **(6)** |  |
|  |  |  |  |  |
|  | **(b)** | State differences between RAM & ROM | **(6)** |  |